UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/717,823	11/20/2003	James R. Krietemeyer	2003P00225US01	1235

7590 06/29/2006

Siemens Corporation
Intellectual Property Department
170 Wood Avenue South
Iselin, NJ 08830

EXAMINER	
SZETO, JACK W	

ART UNIT	PAPER NUMBER
2113	

DATE MAILED: 06/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/717,823	KRIETEMEYER ET AL.	
	Examiner	Art Unit	
	Jack W. Szeto	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/8/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Non-Final Official Action

Status of the Specification and Claims

Claims 1-43 are rejected under 103(a).

Specification is objected to based on minor informalities.

Claim 17 is objected to based on minor informalities.

Claim Objections, Minor Informalities

Claim 17 is objected to because of the following informalities:

As per claim 17, "the numerically controlled machine" is recited, this limitation lack antecedent basis and appropriate corrections are required. There is no "numerically controlled machine tool" recited in the previous claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 4, 6-16, 18, 20-25, 27-43 are rejected under 35 U.S.C. 103(a) as being anticipated by Sutton (United States Patent No 7,047,442) and further in view of STSARCES ("Final Report: Safety-Related Complex Electronic Systems").

As per claim 1, Sutton discloses:

A method, comprising:

automatically enforcing user compliance with a plurality of predetermined steps of a computer-assisted verification test [column 1, lines 5-12: automated test system includes validation test] *of a safety feature* for a machine system [column 1, lines 5-6: complex electronic, electromechanical and mechanical and equipment are machines];

inducing an error condition in the machine system; and

collecting data regarding a response of the machine system *to the error condition* [column 2, lines 38-42: test results (collected data)].

Sutton does not explicitly disclose:

computer-assisted verification *of a safety feature* for a machine system;

inducing an error condition in the machine system;

STSARCES discloses:

computer-assisted verification of a safety feature for a machine system [page 90, ¶4: validating safety of control system];

inducing an error condition in the machine system [page 90, ¶4: fault injection];

Sutton discloses a testing system that can be used to validate the operations of a machine system. However, it is unclear whether these operations includes safety features also. STSARCES primarily focuses on validating safety features in machines system [page 10, ¶1]. Validating safety features is an important task that has big consequences if they are not validated

[page 16 to page 17: dangers of machines]. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate validating of safety features as taught in STSARCES into the testing system of Sutton to create a testing system that encompasses validation of safety features.

Sutton also does not disclose inducing errors into the machines. STSARCES does discloses fault injection into the system for validating safety. Fault injection is a well known method of validation and allows for establishing a close relationship with analytical models [page 90, ¶6]. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to induce error conditions as taught in STSARCES into the testing system of Sutton to create a testing system that establishes a close relationship with analytical models.

As per claim 4, Sutton discloses:

The method of claim 1, further comprising:

providing a user interface for selecting the verification test from a plurality of potential computer-assisted verification tests [column 7, lines 29-33: several procedures are available to user through UI].

As per claim 6, Sutton discloses:

The method of claim 1, further comprising:

receiving a user selection of the verification test from a plurality of potential computer-assisted verification tests [column 7, lines 33-40: plurality of tests].

As per claim 7, Sutton discloses:

The method of claim 1, further comprising:

providing a user interface for selecting a sequential ordering of a plurality of computer-assisted verification tests to perform, the plurality of computer-assisted verification tests comprising the verification test [column 7, lines 29-35: UI provides for selecting of sequential ordered verification tests to perform].

As per claim 8, Sutton discloses:

The method of claim 1, further comprising:

receiving a user selection of a sequential ordering of a plurality of computer-assisted verification tests to perform, the plurality of computer-assisted verification tests comprising the verification test [column 7, lines 29-35: UI accepts the selected of sequential ordered verification tests to perform].

As per claim 9, Sutton discloses:

The method of claim 1, further comprising:

providing a user interface for configuring the verification test [column 8, lines 19-39].

As per claim 10, Sutton discloses:

The method of claim 1, further comprising:

receiving a user-selected configuration for the verification test [column 8, lines 19-39]..

As per claim 11, Sutton discloses:

The method of claim 1, further comprising:

providing instructions for the verification test [Figure 3: help tab].

As per claim 12, Sutton discloses:

The method of claim 1, further comprising:

providing instructional information to a user performing the verification test [Figure 3: help tab].

As per claim 13, Sutton discloses:

The method of claim 1, further comprising:

setting-up one or more initial conditions for the verification test [column 7, lines 55-67: measurements and devices are initially set up].

As per claim 14, Sutton discloses:

The method of claim 1, further comprising:

prompting a user to perform a step from the plurality of predetermined steps of the verification test [column 8, line 23 and Figure 3, reference 306: run button allows user to perform a step].

As per claim 15, Sutton discloses:

The method of claim 1, further comprising:

resetting the error condition [column 8, line 22: reset test].

As per claim 16, Sutton discloses:

The method of claim 1, further comprising:

resetting a data collector [column 8, line 23: reset measurements].

As per claim 18, Sutton discloses:

The method of claim 1, further comprising:

verifying that the verification test succeeded [column 2, lines 45-55: alert if failed or passed results];

As per claim 20, Sutton discloses:

The method of claim 1, further comprising:

monitoring the verification test [column 8, lines 25-39: GUI allows for the status of test to be displayed for the user (monitoring)].

As per claim 21, Sutton discloses:

The method of claim 1, further comprising:

collecting data regarding the plurality of predetermined steps performed during the verification test [column 8, line 33: value of measure displayed (collected)].

As per claim 22, Sutton discloses:

The method of claim 1, further comprising:

collecting data regarding an error condition generated during the verification test [column 10, lines 13-16: find errors in the system].

As per claim 23, Sutton discloses:

The method of claim 1, further comprising:

rendering the collected data [column 8 line 17-39: results (collected data) displayed (rendered)].

As per claim 24, Sutton discloses:

The method of claim 1, further comprising:

analyzing the collected data [column 8, lines 7-13: results are analyzed].

As per claim 25, Sutton discloses:

The method of claim 1, further comprising:

processing the collected data [column 8, lines 7-13: results are processed]

As per claim 27, Sutton discloses:

The method of claim 1, further comprising: merging verification test information with a standardized template to create a report [Figure 3, reference 340: test result displayed in a standard GUI (template)].

As per claim 28, Sutton discloses:

The method of claim 1, further comprising:

generating a report of the verification test [Figure 3, reference 340: test result displayed].

As per claim 29, Sutton discloses:

The method of claim 1, further comprising:

generating a report of the verification test, the report comprising an identity of the verification test performed [Figure 5, reference 502 and column 9, lines 20-57: identity of verification].

As per claim 30, Sutton discloses:

The method of claim 1, further comprising:

generating a report of the verification test, the report comprising an identity of the plurality of predetermined steps [Figure 5 and column 9, lines 20-57: identity of the steps (test) preformed].

As per claim 31, Sutton discloses:

The method of claim 1, further comprising:

generating a report of the verification test, the report comprising a description of the plurality of predetermined steps [Figure 5 and column 9, lines 20-57: title is a description of the steps (test) preformed].

As per claim 32, Sutton discloses:

The method of claim 1, further comprising:

generating a report of the verification test, the report comprising initial conditions [column 7, lines 55-67 and lines 28-35: the measurements are initially configure and displayed in the report].

As per claim 33, Sutton discloses:

The method of claim 1, further comprising:

generating a report of the verification test, the report comprising the error condition induced [column 10, lines 13-33: error conditions induced by the test are included results].

As per claim 34, Sutton discloses:

The method of claim 1, further comprising:

generating a report of the verification test, the report comprising the data collected [column 8, lines 40-67: collected data reported].

As per claim 35, Sutton discloses:

The method of claim 1, further comprising:

generating a report of the verification test, the report comprising analysis of the collected data [column 8, lines 40-67: analysis of the collected data is reported].

As per claim 36, Sutton discloses:

The method of claim 1, wherein user compliance is enforced via a graphical user interface [column 8, line 19].

As per claim 37, Sutton discloses:

The method of claim 1, wherein the collected data comprise status data [column 8, lines 35-39].

As per claim 38. , Sutton discloses:

The method of claim 1, wherein the collected data comprise alarm data [column 6, lines 35-45: alerts are collected and provided to the user].

As per claim 39, Sutton discloses:

The method of claim 1, wherein the collected data comprise a trace [Figure 4 and lines 40-46: progress windows plots datapoints against the progress axis (time)].

As per claim 40, STSARCES discloses:

The method of claim 1, wherein the machine system comprises a machine tool [page 12, ¶1: machine comprises a tool which can be changed or maintained].

As per claim 41, STSARCES discloses:

The method of claim 1, wherein the machine system comprises a numerical controller [page 12, ¶4: numerically controlled machine].

Claim 42 contains the same subject matter as claim 1. Thus claim 1 will be used as an example rejection for claim 42.

Claim 43 contains the same subject matter as claim 1. Thus claim 1 will be used as an example rejection for 43.

Claims 2-3 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sutton (United States Patent No. 7,047,442) and STSARCES ("Final Report: Safety-Related Complex Electronic Systems"), and further in view of Tracy (United States Patent No. 6,901,346).

As per claim 2, Tracy discloses:

The method of claim 1, further comprising: providing a user interface for selecting a stage of development for the machine system [column 5, lines 26-30: version field (stage of development)].

As per claim 3, Tracy discloses:

The method of claim 1, further comprising: receiving a user selection of a stage of development for the machine system [column 5, lines 26-30: version field (stage of development)].

As per claim 5, Tracy discloses:

The method of claim 1, further comprising:

providing a user interface for selecting the verification test from a plurality of potential computer-assisted verification tests, the plurality of potential computer-assisted verification tests limited by a stage of development of the machine system [column 10, lines 37-45: based on the information provided, pertinent aspects of the requirement is used to build a traceability matrix for C&A (verification)].

While neither Sutton nor STSARCES explicitly discloses a testing system where a stage of development for the system is provided and accepted then used to determine verification tests, STSARCES does explicitly state testing the system during all phases of development [STSARCES, page 19, ¶4]. Having an interface to provide and accept the stage of development and then fine tuning the test cases accordingly allows for more robust system as testing/verification is done at throughout the systems lifecycle [STSARCES, page 19, ¶4]. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate having a user interface to provide and accept a stage of development for a system and then tune the test cases accordingly as taught in Tracy into the testing system of Sutton to create a testing system which increase the robustness of the system being tested.

Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sutton (United States Patent No. 7,047,442) and STSARCES ("Final Report: Safety-Related Complex Electronic Systems"), and further in view of Niwa (United States Patent No. 6,397,111).

As per claim 17, Niwa discloses:

The method of claim 1, further comprising:

placing the numerically controlled machine tool in a test mode [column 18, lines 34-37];

While neither Sutton nor STSARCES explicitly discloses a testing system where the NC machine tool is placed in a test mode, placing systems in test mode before testing is common and well known in the art as illustrated in Niwa. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to place the machine tool in a test mode as taught in Niwa into the testing system of Sutton to create a testing system.

Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sutton (United States Patent No. 7,047,442) and STSARCES ("Final Report: Safety-Related Complex Electronic Systems"), and further in view of Brayton (United States Patent Publication No. 2004/0064253).

As per claim 19, Brayton discloses:

The method of claim 1, further comprising:

facilitating human verification that the verification test succeeded [para 0036: operator is asked to manually verify certain steps of the test].

Sutton, STSARCES, and Brayton disclose testing systems. However, neither Sutton nor STSARCES disclose whether human verification is included in the verification test. Human verification is well known in the art and allows for flexibility in testing. Certain tests cannot be verified automatically and requires manual intervention [para 0036: perform a function which requires manual intervention]. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate human verification as taught in Brayton into the testing system of Sutton and STSARCES to create a more flexible testing system.

Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sutton (United States Patent No. 7,047,442) and STSARCES ("Final Report: Safety-Related Complex Electronic Systems"), and further in view of Thompson (United States Patent No. 5,247,664).

As per claim 26, Thompson discloses:

The method of claim 1, further comprising:

updating a status of the verification test after correction of a problem [column 2, lines 15-21: status is changed after correction of the fault].

Neither STSARCES nor Sutton's testing system discloses updating the status of the verification test after correction the problem. On the other hand, Thompson explicitly discloses updating the status of the test after correcting the problem. Updating the status after a correction allows the system to continue on its processing [column 2, lines 17-21]. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to updating the status after

a correction is implemented as taught in Thompson into the testing system of Sutton and STSARCES to a testing system which allows for the continuing processing.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jack W. Szeto whose telephone number is (571) 272-1537. The examiner can normally be reached on M-F 8 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jws

Bryce P. Bonzo

BRYCE P. BONZO
PRIMARY EXAMINER